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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,805	03/09/2004	Hussein I. Hanafi	YOR920030374US1 (16927)	8140
7590	11/09/2005		EXAMINER	
Steven Fischman, Scully, Scott, Murphy & Presser 400 Garden City Plaza Garden City, NY 11530			LIN, SUN J	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/796,805

Applicant(s)

HANAFI ET AL.

Examiner

Sun J. Lin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04/01/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. This office action is in response to application 10/796,805 filed on 03/09/2004.
Claims 1 – 13 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:
- Claim 1, line 1, after “roll-off” insert **—within a semiconductor chip or system—**.
 - Claim 1, line 3, before “channel” delete **—the—**.
 - Claim 1, line 6, after “transistor” insert **—device—**.
 - Claim 1, line 6, before “threshold” insert **—its—**.
 - Claim 1, line 7, before “off-current” delete **—the—**.
 - Claim 1, line 8, change “the back-gate” to **—back gate—**.
 - Claim 1, line 8, before “body” delete **—the—**.
 - Claim 1, line 8, change “devices that have” to **—devices, each of which has—**.
 - Claim 1, line 9, after “I-off_{max}” insert **— , —**.
 - Claim 1, line 9 – 10, change “the threshold voltage” to **—threshold voltage of each of said some transistor devices—**.
 - Claim 1, line 10, after “compensating” insert **—the—**.
 - Claim 3, line 1, change “off-current setting” to **—setting off-current—**.
 - Claim 4, line 2, after “5” insert **—keV—**.
 - Claim 5, line 2, after “1E11” insert **—atoms/cm³—**.
 - Claim 6, line 2, after “1E11” insert **—atoms/cm³—**.
 - Claim 9, line 2, before “testing” insert **—the—**.
 - Claim 10, line 2, before “testing” insert **—the—**.
 - Claim 12, line 2, change “back gate” to **—back gate—**.
 - Claim 12, line 2, change “node” to **—nodes—**.
 - Claim 12, line 2, change “second” to **—some—**.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- (1). Determining the scope and contents of the prior art.
- (2). Ascertaining the differences between the prior art and the claims at issue.
- (3). Resolving the level of ordinary skill in the pertinent art.
- (4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 2 and 9 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,472,919 B1 to Burr in view of U.S. Patent No. 4,542,485 to Iwahashi et al.

5. As to Claim 1, Burr shows and discloses the following subject matter:

- A computer system having many ultra-low voltage latches, which are made up of a plurality of transistor devices – [col. 1, line 6 – 47];
- Threshold voltage roll-off effect of a transistor (device) – [Fig. 2B];
- Threshold voltage of a transistor is dependent on channel length (of the transistor) – [col. Lin 27 – 29]; Transistors with shorter channel lengths have different threshold voltages than the transistors with longer channel length due to threshold voltage roll-off effect – [col. 8, line 59 – 61; Fig. 2B]; Notice that a nominal transistor device is designed to have a nominally uniform threshold voltage $V_{t_{nom}}$ when channel length is equal to L_{nom} (i.e., nominally channel length)
- Off-current I_{off} (i.e., leakage current) of a transistor (device) is dependent and affected by threshold voltage of the transistor (device)...variations in threshold voltage due to processing variations (in manufacturing transistor devices), the exact dopant concentration (e.g., implanating) in each channel (of a transistor device) can vary slightly from transistor device to transistor device – [col. 6, line 42 – 60];
- Low threshold transistors and voltage scalability of latches – [abstract]; Threshold voltage versus effective channel length of a transistor using halo

channel doping – [Cure 260 in Fig. 2B; col. 6, line 61 – col. 7, line 25]; It is noticed in curve 260 of Fig. 2B that (1) maximum allowable off-current (i.e., $I_{\text{off}_{\text{max}}}$) can be specified to associate with a maximum achievable channel length, which is equal to L_{max} , in transistor manufacturing process (2) a minimum threshold voltage $V_{t_{\text{min}}}$ can be achieved using halo channel doping, which implanting appropriate ions in each channel of each transistor (device) to adjust its channel length within an acceptable range; Also notice that off-current (leakage current) of each transistor device installed in the computer system can be verified (i.e., tested and measured) in QC step after manufacturing of the computer system (i.e., after installing the transistor devices in the computer system).

In addition to using halo channel doping to control threshold voltage of a transistor device, Burr also discloses and lists a set of U.S. Patents on biasing back gate of a transistor device to tune/control its threshold voltage – [col. 11, line 32 – col. 12, line 17]. Burr does not explicitly teach a method of biasing back gate of a transistor in order to increase threshold voltage to about $V_{t_{\text{min}}}$ thereby compensating the threshold voltage roll-off of the transistor. But Iwahashi et al. teach applying back gate bias to a MOS transistor to an extent as to compensate for dropped (i.e., roll-off) amount of the threshold voltage V_{TH} – [col. 9, line 20 – 36]. Notice that applying back gate bias to some transistor devices that do not meet a pre-selected specification on $I_{\text{off}_{\text{max}}}$ (maximum allowable leakage current) installed in a computer system in order to compensate for threshold voltage roll-off of those transistor devices thereby minimizing the overall leakage current of the computer system.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Iwahashi et al. in applying back gate bias to some transistor devices that do not meet a pre-selected specification on $I_{\text{off}_{\text{max}}}$ (maximum allowable leakage current) installed in a computer system in order to compensate for threshold voltage roll-off of those transistor devices thereby minimizing the overall leakage current of the computer system.

For reference purposes, the explanations given above in response to Claim 1 are called [Response A] hereinafter.

6. As to Claim 2, it is well known in the art that nominal channel length L_{nom} of a transistor (device) is achieved based on technology and material utilized in manufacturing the transistor (device). $L_{nom} = 25$ nm is achievable in manufacturing of a MSDFET.

7. As to Claims 9 and 10, reasons are included in [Response A] given above. Notice that the (back gate) biasing can be performed during the testing or after the testing of off-current of each transistor device installed in the manufactured computer system.

8. As to Claims 11 – 13, Iwahashi et al. show and teach that suitable back gate bias is provided by an source potential V_c using an internal (power divider) circuit – [Fig. 8; col. 9, line 20 – 36]. Notice that, as long as voltage value is suitable, the back gate bias can also be provided by any voltage supply elements, including an external DC voltage source (See U.S. Patent 4,260,909 to Dumbri et al.; abstract) or an external clock system that can deliver a potential (See U.S. Patent 6,023,641 to Thompson; col. 8, line 47 – col. 9, line 5).

9. Claims 3 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,472,919 B1 to Burr and U.S. Patent No. 4,542,485 to Iwahashi et al. in view of U. S. Patent No. 5,622,880 to Burr et al. (called Burr2 et al. hereinafter).

10. As to Claim 3, Burr and Iwahashi et al. (called Burr & Iwahashi hereinafter) show and disclose all subjected recited in Claim 1, Burr also discloses that off-current of a transistor device is dependent on its threshold voltage. Burr & Iwahashi do not teach that setting the off-current of a transistor is controlled by varying implant conditions and ion dosage. But Burr2 et al. teach choosing (varying) formation conditions (i.e., implanting conditions) and dopant concentration (i.e., ion dosage) of channel region of a MOSFET transistor to control its threshold voltage – [col. 8, line 64 – col. 67; col. 10, line 61 – col. 12, line 54]. Notice that choosing (varying) formation conditions (i.e., implanting conditions) and dopant concentration (i.e., ion dosage) for forming channel region of a transistor device is to control/adjust threshold voltage of the transistor device in order to determine a maximum allowable off-current $I_{off_{max}}$.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Burr2 et al. in choosing (varying) formation conditions and dopant concentration for forming channel region of a transistor device in order to control/adjust threshold voltage of the transistor device thereby determining a maximum allowable off-current **I-off_{max}**.

11. As to Claims 4 – 8, Burr2 et al. disclose the following subject matter:

- Implanting is performed at an energy of between about 10 – 30 keV – [col. 11, line 13 – 32];
- Ion dosage for a p-type dopant (boron) is from 5×10^{11} to 5×10^{12} atoms/cm² – [col. 11, line 50 – 59]; Notice that boron is an element in Group III;
- Ion dosage for a n-type dopant (P, As, Sb or Sn) is from 10^{13} – 10^{14} atoms/cm² – [col. 12, line 38 – 54]; Notice that P, As, Sb and Sn are elements in Group V.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
November 7, 2005

